AMENDMENT TRANSMITTAL LETTER

Docket No.
M4065.0176/P176

Application No.	Filing Date	Examiner	Art Unit
09/354,302	July 16, 1999	A. Luu	2816

Applicant(s): Christopher K. Morzano

Invention: APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	98	- 98 =		x	0.00
Independent Claims	10	- 10 =		x	0.00
Multiple Dependent Claims (check if applicable)	☐				
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00

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Dated: March 11, 2002

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#14/Response

Docket No.: 99-0080
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

3/12/02

In re Patent Application of:
Christopher Morzano

Serial No.: 09/354,302 Group Art Unit: 2816

Filed: July 16, 1999 Examiner: A. Luu

For: APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

REMARKS/ARGUMENTS

The application has been carefully reviewed in light of the Office Action dated December 11, 2001 (Paper No. 13). Claims 38-56 are allowed. Claims 1-56 and 82-98 are now pending in this case.

Claims 1-7, 16-19, 82 and 86-90 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Makihara et al, U.S. Patent No. 5,243,573 (hereinafter "Makihara"). The rejection is respectfully traversed.

The present invention is an apparatus and method for adjusting clock skew. To reduce the clock skew, a non-inverted clock signal ("CLK") and an inverted clock signal ("XCLK") are connected to back-to-back inverters. The signal that takes longer to switch states has an extra inverter driving it when it switches states and the signal that switches states faster has an extra inverter fighting it when it switches states so that the resulting output signals are in the same state for a shorter period of time and the clock skew is

reduced. When the input signals CLK and XCLK are not switching and are in opposite states, this circuit does not affect the output signals.

Makihara, however, is a is a circuit which senses the logic level of data signals output from a memory array. Unlike the present invention which receives two complementary clock signals as inputs and adjusts them to reduce the skew between them, Makihara senses the difference between a data signal and a reference data signal and outputs the recognized signal and its complement on two output lines. Figure 2, cited by the Examiner, uses the outputs at nodes N4 and N5 to supply a data signal and its complement.

Claims 1 and 16 recite input/output lines that receive and output complementary clock signals. Makihara does not receive complementary clock signals as input signals, nor does it output complementary clocks signals. Amended Claim 1 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals." If clock signals were input into the circuit recited in Makihara, the skew of the signals would not be reduced. Instead, the output would be a detection of and amplification of the difference between the two input signals. Makihara, therefore, does not recite all of the elements of amended Claim 1. Accordingly, amended Claim 1 is now in condition for allowance.

Claims 2-7 depend from amended Claim 1. For at least the reasons discussed above in reference to amended Claim 1, Claims 2-3 and 6-7 are allowable along with amended Claim 1.

Amended Claim 16 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals." Claim 16, like Claim 1, recites receiving and outputting complementary clock signals. Accordingly, for at least the reasons discussed above with reference to amended Claim 1, amended Claim 16 is

patentable over Makihara.

Claims 17-19 depend from amended Claim 16. Therefore, Claims 17-19 now include the same limitations as Claim 16. For at least the reasons discussed above in reference to amended Claim 16, Claims 17-19 are allowable along with amended Claim 16.

Claim 82 recites "receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal." Makihara does not disclose or suggest a circuit which receives such clock signals. Thus, Claim 82, like Claim 1, is not anticipated by Makihara. Accordingly, for at least the reasons discussed above in reference to amended Claim 1, Claim 82 is also patentable over Makihara.

Claims 86-90 depend from claim 82. Accordingly, for at least the reasons discussed above with reference to Claim 82, Claims 86-90 are allowable along with Claim 82.

Claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Makihara in view of Garcia, U.S. Patent No. 5,949,259 (hereinafter "Garcia"). The rejection is respectfully traversed.

Claims 8 and 11-13 depend from Claim 1. As noted, Claim 1 recites "at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals," a feature not disclosed in Makihara. Garcia teaches a zero-delay slew-rate controlled output buffer. The circuit described in Garcia does not receive or output complementary clock signals. Accordingly, neither of the cited references teach or suggest the claimed invention. For at least the foregoing reasons, Claims 8 and 11-13 are patentable over Makihara in view of Garcia.

Claims 20 and 23-25 depend from Claim 16. Therefore, Claims 20 and 23-25 include the same limitations as Claim 16. Claim 16 recites "at least a first and second complementary clock signal input/output line for receiving first and second

complementary clock input signals and transmitting first and second complementary clock output signals." Applicant previously noted that Makihara does not teach or suggest this aspect of the invention. Garcia is similarly deficient. For at least the reasons discussed above in reference to amended Claim 16, Claims 20 and 23-25 are allowable along with amended Claim 16.

Claim 26 recites similar limitations to amended Claim 16. For at least the reasons discussed above with reference to Claim 16, Claim 26 is allowable along with amended Claim 16.

Claims 27-33 and 36-37 depend from amended Claim 26 and are allowable for the reasons discussed above with reference to Claim 26.

Claims 83-86 depend from Claim 82 and are allowable for the reasons discussed above with reference to Claim 82.

Claim 91 recites "receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal." Neither Makihara nor Garcia teach this aspect of the claimed invention. Accordingly, Claim 91 is also in condition for allowance.

Claims 92-98 depend from Claim 91 and are allowable for the reasons discussed above with reference to Claim 91.

Claims 9-10, 21-22 and 34-35 are objected to as being dependent upon a rejected base claim.

The rejections to the independent claims upon which Claims 9-10, 21-22 and 34-35 are based have been addressed. Applicant believes that these independent claims are in condition for allowance. Accordingly, Claims 9-10, 21-22 and 34-35 are also in condition for allowance.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: March 11, 2002

Respectfully submitted,

By_____

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